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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 102-0118US2

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on May 17, 2006

Signature: Stephanie E Davis

Typed or printed name: Stephanie Davis

Application Number	Filed
09/740,751	December 19, 2000

First Named Inventor: Tongbi Jiang

Art Unit	Examiner
3729	Rick K. Chang

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☒ attorney or agent of record. Registration number 46,065
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34

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May 17, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Tongbi Jiang and Zhiqiang Wu

Assignee: Micron Technology

Serial No.: 09/740,751

Filed: December 19, 2000

Title: Method for Forming Novel Zero Force Insertion Sockets Using Negative Thermal Expansion Materials *(as amended previously)*

Group Art Unit: 3729

Examiner: Rick K. Chang

Examiner phone: (703) 308-4784

Atty. Dkt. No.: 102-0118US2

ARGUMENTS ACCOMPANYING PRE-APPEAL BRIEF REQUEST FOR REVIEW

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Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Applicants submit this Pre-Appeal Brief for consideration in this application pursuant to the procedure as promulgated on July 12, 2005 in the Official Gazette, and as extended pursuant to the notice of January 10, 2006 in the Official Gazette.

This brief is filed concurrently with a Notice of Appeal.

This Office is authorized to deduct any necessary fees, including any extension of time fees, from Deposit Acct. 50-1922.

Pending independent claims 18 and 47,[1] recited below for convenience, claim a method for forming a socket for receiving at least one terminal pin of an electronic component. As can be seen in the claims, the claimed socket comprises a second material stacked on a first material. The coefficients of thermal expansion are different for the two materials. As recited in each claim, "[the] first material has a positive coefficient of thermal expansion and ***[the] second material has a negative coefficient of thermal expansion***." In other words, the second material is non-traditional in that it contracts with increasing temperatures (negative CTE) as opposed to more-traditional first materials that expand with increasing temperatures (positive CTE).

18. A method of forming a socket for receiving a terminal pin from an electronic component therein, comprising:
forming a layer of a first material on an upper surface of a substrate; and
forming a layer of a second material on said layer of said first material;
wherein said first and second layers comprise an aperture to expose said upper surface of said substrate, and
wherein said first material has a positive coefficient of thermal expansion and said ***second material has a negative coefficient of thermal expansion.***

47. A method of forming a socket having at least one electrical contact, the socket for bringing at least one terminal pin of an electronic component into contact with an electrical contact, comprising:
forming a first material on a substrate, the first material comprising a first aperture for receiving the terminal pin, wherein the first aperture exposes an electrical contact associated with the substrate; and
forming a second material on the first material, the second material comprising a second aperture for receiving the terminal pin, wherein the second aperture is concentric with the first aperture;
wherein the first material has a positive coefficient of thermal expansion and the ***second material has a negative coefficient of thermal expansion.***

In the Final Office action dated February 28, 2006, claims 18 and 47 were again rejected by the Examiner for obviousness given the combination of USP 4,642,160 ("Burgess") with USP 4,513,055 ("Leibowitz").

Burgess, the primary reference relied upon by the Examiner, discloses a traditional printed circuit board (PCB) and method of its manufacture. The Examiner

[1] Claims 18 and 47 are the only pending independent claims. Other independent claims in the application currently stand withdrawn due to an earlier election of species requirement.

contends that Burgess discloses all of the limitations of claims 18 and 47, except the above-highlighted limitation of a second material having a negative coefficient of thermal expansion (CTE). Specifically, the Examiner contends that Burgess's bonding sheet 16 (an insulator) comprises Applicant's claimed first material; that copper foil 18 comprises Applicant's claimed second material; and that aperture 28 comprises Applicant's claimed aperture formed in both the first and second materials (see Fig. 7 of Burgess). In other words, the Examiner finds all of the limitations of claims 18 and 47 in Burgess, ***except that Burgess's copper layer 18 (i.e., the second material) does not have a negative CTE.***

However, ***the Examiner contends that Leibowitz contains this missing limitation.*** Specifically, Leibowitz discloses a composite layer 10 useable in a printed circuit board comprising a fabric 14 formed in a resin 16 (see Fig. 2). The fabric 14 in turn is composed of two yarns 18 and 20 "having positive and negative coefficients of thermal expansion, respectively." Col. 3, ll. 58-59. The negative coefficient yarn 20 can comprise Kevlar. See col. 3, ll. 30-31.

Clear Error #1: The Examiner is Incorrect that Leibowitz discloses a Negative CTE Material for a Socket as Claimed

To reiterate, the limitation from claims 18 and 47 lacking from the primary reference (Burgess) is a second material for a socket having "***a negative coefficient of thermal expansion***." The Examiner contends this material is present in Leibowitz

The Examiner is not clear which material in Leibowitz he considers to correspond to this claim limitation. On the one hand, the Examiner cites specifically to col. 3, ll. 20-21, which discusses only the negative-CTE Kevlar yarn 20. Office Action at pg. 2, ¶ 2. But later the Examiner cites to col. 6, ll. 1-10, which discuses the overall composite 10. Office Action at pg. 5, ¶ 8.

One of ordinary skill in the art would clearly understand that only the composite material 10 (which contains the yarn 20) could correspond to this claim limitation for a material for a socket. Only composite 10 is disclosed as having suitable rigidity etc. to possibly function as the material for a socket. By contrast, the negative-CTE (Kevlar) yarn 20 could not—by itself—function as the material for the socket: flexible yarns would not be understood by one of ordinary skill as suitable by themselves for use as a material for a socket.

When it is understood that only Leibowitz's composite 10 could possibly comprise the claimed second material, it is useful to understand more about the function of this material in Leibowitz's disclosure. The stated goal of Leibowitz is to form a PCB with a CTE that matches the typically-lower positive CTEs of the material of ceramic chip carriers that will be mounted on the PCB. See col. 2, ll. 6-10; col. 5, ll. 35-40. Matching the CTEs of the materials for the chip carriers (e.g., aluminum oxide) with the CTE for the PCB prevents the two from cracking at their boundary. Col. 1, ll. 45-53. To achieve the goal of lowering the CTE of the PCB, Leibowitz proposes his composite 10. See col. 2, ll. 19-39. As noted above, the composite 10 incorporates negative-CTE yarn 20 in conjunction with other positive-CTE materials such as yarn 18 and resin 16. The effect is that the CTE for the PCB is lowered and is hopefully brought to the same level as the CTE for the material of the chip carriers, thus preventing thermal mismatch. Col. 3, ll. 37-48. Indeed, Leibowitz notes that the proportion of the negative-CTE yarn 20 and the positive-CTE yarn 18 can be changed to modify the CTE of the composite. Col. 2, ll. 27-33; col. 6, ll. 1-8.

But the overall composite 10 is expressly disclosed in Leibowitz as having a positive coefficient of thermal expansion. See, e.g., Col. 1, ll. 33-39 (discussing a composite having a positive CTE matching the CTE of aluminum oxide used in the chip carriers); Col. 5, ll. 7-21. This is not surprising because the ceramic chips to be mounted on these boards (and to which thermal matching is desired) also exhibit a positive coefficient. In other words, while Leibowitz discloses using a negative-CTE yarn 20 to reduce the CTE of the composite 10, ***nowhere is it disclosed or suggested that the use of a negative-CTE yarn 20 yields a negative-CTE composite 10***. Indeed, a negative-CTE composite would be counter to Leibowitz's stated purpose, which is to provide a composite with a CTE that essentially matches the positive CTE of the material (aluminum oxide) of the chip carriers. Therefore, while the Examiner notes that the "ratio of the positive and negative CTE [yarns] can be varied as desired," Office Action at pg. 5, ¶ 8, the Examiner fails to notice that such variations are disclosed in Leibowitz as only yielding a composite 10 which has a positive CTE. It is ***NEVER*** disclosed or suggested in Leibowitz that his technique can be used to yield a composite 10 which has a negative CTE, and again as such would be counterintuitive to Leibowitz's stated goal of

reducing thermal mismatch with the ceramic chip carriers. See also col. 2, ll. 27-33 (noting that the resin 16 and the copper in the finished circuit board also affect the overall CTE of the composite).

The relevant point is that Leibowitz does not disclose or suggest a material useable in a socket and which has a negative CTE as claimed. Because neither Leibowitz nor Burgess discloses or suggest this limitation, the combination of the references fails to disclose all of the claim limitations and hence cannot render claims 18 and 47 obvious as a matter of law. See MPEP § 2143.03.

Clear Error #2: The Combination of Burgess and Leibowitz Yields an Inoperative Combination, and Hence the Examiner is Wrong in Concluding that Suggestion or Motivation Exists to Combine These References

A further reason exists for why claims 18 and 47 are clearly not rendered obvious by Burgess and Leibowitz, and such further reason shows that the Examiner is incorrect in concluding that one of ordinary skill in the art would have been motivated to have modified Burgess in light of Leibowitz.

The Examiner assumes that the second material in Burgess's PCB—copper layer 18—could simply by modified to comprise a negative CTE material such as that disclosed in Leibowitz. Burgess's copper layer 18 is a ***conductive material*** which is etched to form conductive traces to carry various signals on Burgess's PCB. See col. 5, ll. 21-24 (noting that copper foil 18 is eventually etched to define "conductor runs 40" as shown in Fig. 9).

Whether the relevant "second material" in Leibowitz is considered the negative-CTE Kevlar yarn 20 itself or the composite 10, ***the fact remains that the relevant material in Leibowitz is clearly an insulating material.*** Indeed, the composite layer 10 is specifically used in Leibowitz's PCB as the insulator between copper layers 22 (see Fig. 3).

Therefore, the Examiner's position is that one of ordinary skill in the art would be suggested or motivated to exchange the copper layer 18 in Burgess's PCB with a suitable material from Leibowitz—either the yarn 20 or composite 10. In short, ***the Examiner contends that one of ordinary skill in the art would be motivated to exchange the***

conductive traces on Burgess's PCB with insulting materials from Leibowitz that are clearly incapable of conducting current.

This reasoning yields an ***inoperable structure***—i.e., a printed circuit board with non-conductive traces. As the Examiner is well aware, a theory for suggestion/motivation to combine various prior art references that results in an inoperable structure cannot be legally sustained. See MPEP § 2143.01 ("If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification."). Therefore, for this additional reason, neither claims 18 nor 47 are obvious given the combination of Burgess and Leibowitz. Simply put, the Examiner is clearly incorrect to reason that one of ordinary skill in the art would be suggested or motivated to modify Burgess's PCB to incorporate insulating materials from Leibowitz that would render Burgess's PCB unsatisfactory for its intended purpose.

* * * * *

The Applicant submits that claims 18 and 47 are patentable over Burgess and Leibowitz, and therefore that claims dependent thereon are also necessarily patentable. It is therefore requested that the obviousness rejection of these claims be lifted, and that prosecution continue as to the currently-withdrawn claims.

Please feel free to contact the undersigned with any questions relating to this submission.

Respectfully submitted,

May 17, 2006
Date

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